PRO-LOG® CORPORATION

STD 7000

7805
8085A Processor Card

USER'S MANUAL

1/83

FOREWORD

This manual explains how to use Pro-Log's 7805 Processor Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7805. We welcome your suggestions on how we can improve our instructions.

The 7805 is part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of utilizing his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find Pro-Log's *Microprocessor User's Guide* and the *Series 7000 STD BUS Technical Manual* to be useful documents in your work. If you would like a copy of these publications, please submit your request on your company letterhead.

Contents

	Page
FOREWORD	ii
FIGURES	iv
SECTION 1—Purpose and Main Features	1-1
SECTION 2—Installation and Specifications	2-1
Introduction	2-1
Jumper Options	2-1
Memory Mapping	2-4
Memory Types	2-6
MEMEX	2-6
IOEXP	2-6
J1 16-Pin DIP Socket	2-6
Timing Specifications	2-7
Power-on and Push-button Reset	2-10
Specifications	2-11
SECTION 3—Operation and Programming	3-1
SECTION 4—Operating Software	4-1
SECTION 5—Maintenance	5-1
Return for Repair Procedures	5-2

Figures

Figure		Page
1-1	7805 Processor Card	1-1
1-2	Block Diagram	1-2
2-1	Installation of the 7805 in STD BUS Card Rack	2-1
2-2	Jumper Locations and Functions	2-2
2-3	Chip Disable Jumpers	2-3
2-4	Wire Jumper Replacements	2-3
2-5	Memory Addressing Options	2-5
2-6	Suggested Memory Devices	2-6
2-7	The J1 16-Pin DIP Socket	2-7
2-8	Load Characteristics and Pinouts for the J1 Connector	2-7
2-9	Reset After Power-up	2-7
2-10	BUS Request Timing	2-8
2-11	Wait Request Timing	2-8
2-12	Write Timing: Memory Write and Output	2-9
2-13	Read Timing: Memory Read, Input and Interrupt	2-10
2-14	Electrical Specifications	2-11
2-15	Environmental Specifications	2-11
2-16	Electrical Specifications Over Operating Range	2-11
2-17	STD BUS Edge Connector Pin List	2-12

SECTION 1
Purpose and Main Features

PURPOSE

The 7805 Processor Card combines a buffered and fully expandable 8085A microprocessor with a 2K byte-wide CMOS RAM and sockets for an additional 2K bytes of RAM and 8K bytes of EPROM or ROM (2716 type).

A connector is provided to allow access to the 7.5, 6.5 and 5.5 interrupt pins as well as the serial input data (SID) and serial output data (SOD) pins on the processor.

The 7805 (see Figures 1-1 and 1-2) provides all control signals necessary to fully expand the 8085A microprocessor. Also featured is an option of two clock speeds: a 6.144MHz crystal producing 325.5ns ±0.05% time states with the 7805-1 or a 6.25MHz crystal producing 320ns ±0.05% time states with the 7805-0.

The 7805 responds to the STD BUS signal BUSRQ* allowing direct memory access (DMA) to other cards used in the system.

FEATURES

- 4096 bytes RAM capacity onboard
- 2048 bytes RAM included (static CMOS byte-wide type)
- 8192 bytes EPROM capacity onboard (2716 type)
- 3-state address, data and control buses
- Power supply-independent reset circuit
- Five interrupts
- 8085A SID and SOD lines accessible
- Single +5V operation

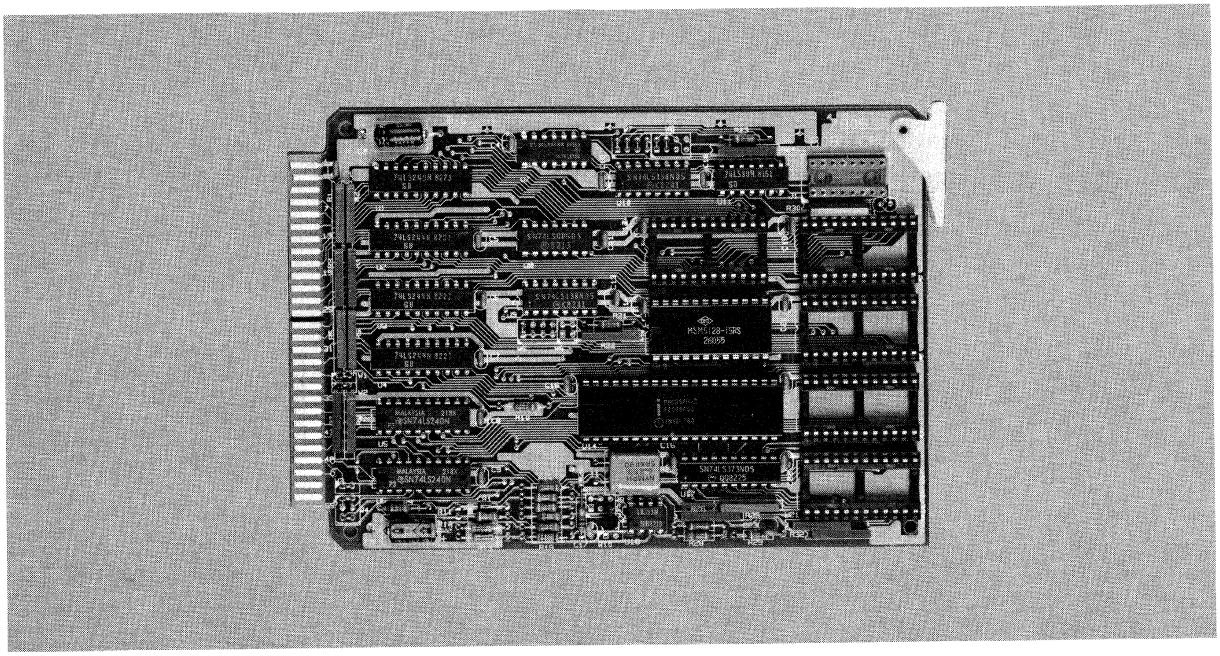


Figure 1-1. 7805 Processor Card

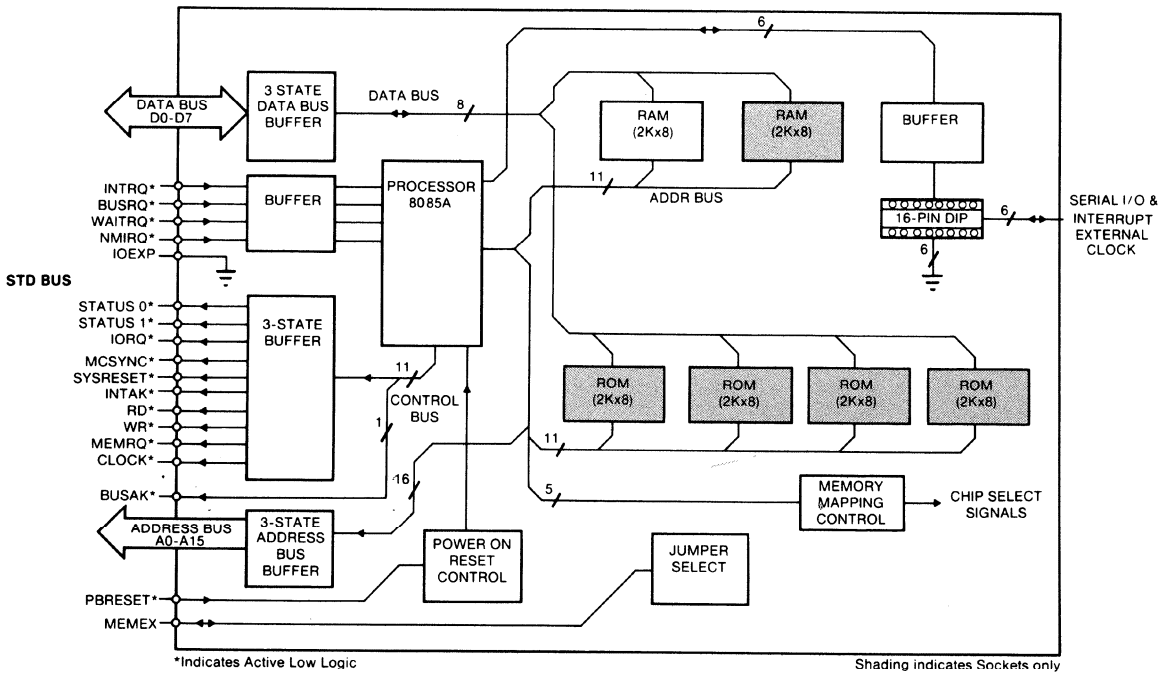


Figure 1-2. Block Diagram (7805)

SECTION 2
Installation and Specifications

INTRODUCTION

The 7805 Processor Card operates as an integral part of an STD BUS system. It may be inserted directly into the STD BUS backplane (see Figure 2-1) or extended from the motherboard with a 7901 Utility Card Extender.

The 7805 can be inserted directly into any available slot in the STD BUS card rack. If the 7901 card is utilized, insert it in any available slot in the card rack and then insert the 7805 into the connector on the 7901 card. This now makes the 7805 accessible for testing.

JUMPER OPTIONS

The 7805 has several optional functions which are selectable by wire jumpers. Figures 2-2 and 2-3 show the locations and the functions of these jumpers. After reviewing the jumper options available, check to be certain the card is properly configured to your specific applications before installing it in the system.

These jumpers can be disconnected simply by cutting them. Be sure to cut them in two places to prevent them from reshorting. To replace a jumper, cut in half and remove one half at a time. Remove any excess solder and install new jumpers as needed.

If there is a need to frequently change these jumpers (e.g. in prototyping), you may want to replace these wire jumpers with slip-on connectors. Permanent 0.025 inch square posts can be installed which will accept the slip-on connectors. Figure 2-4 provides a list of part numbers for these jumper replacements.

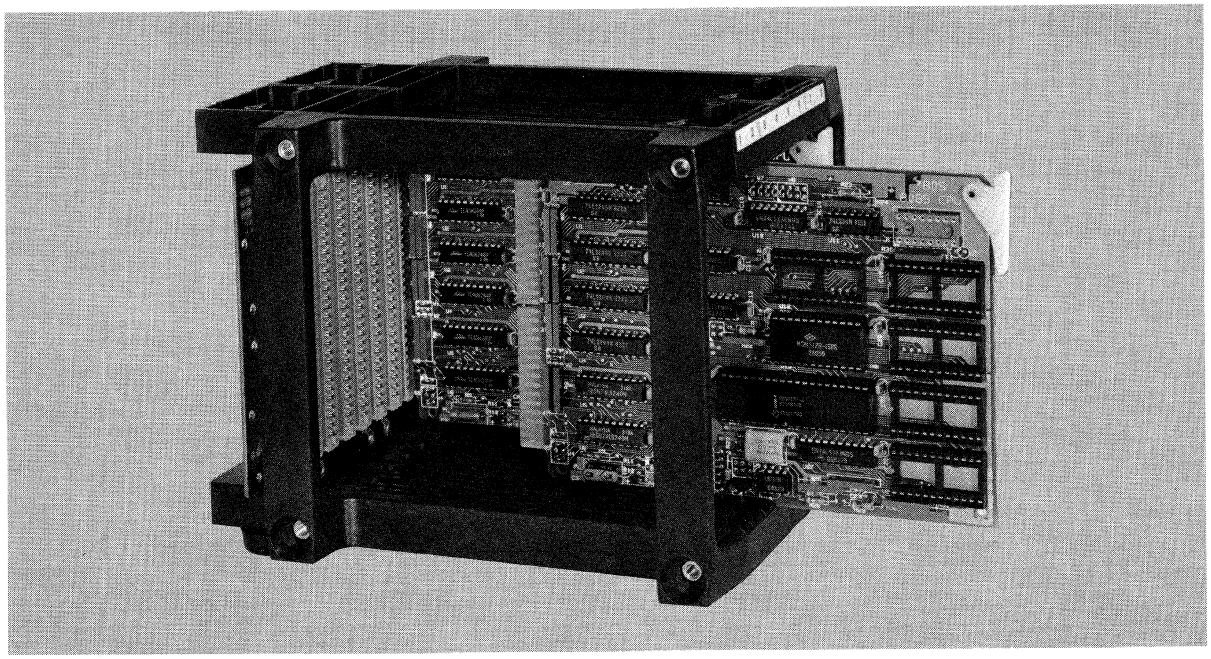


Figure 2-1. Installation of the 7805 in STD BUS Card Rack

W1	1-2 no jumper	=STD BUS MEMEX line grounded =STD BUS MEMEX left floating to be controlled by another card
W2	1-2 no jumper	=STD BUS IOEXP line grounded =STD IOEXP line left floating to be controlled by another card
W3	1-2 no jumper	=8085A clock driven onto STD BUS CLOCK* line =STD BUS CLOCK* line pulled up
W4	1-2 & 5-6	=STD BUS INTRQ* line connected to INT input of 8085A, and external interrupt input J1-3 connected to 8085A interrupt input RS 5.5
	3-4	=STD BUS INTRQ* line connected to 8085A interrupt input RS 5.5, and external interrupt input J1-3 not connected
W5		Selects card address range (see Figure 2-5)

W6	1-2 3-4 no jumper	=Onboard memory enabled with MEMEX high =Onboard memory enabled with MEMEX low =Onboard memory permanently enabled
W7		Each removed jumper disables one EPROM socket (see Figure 2-3)
W8		Affects RAM memory mapping (see Figure 2-5) Also used to disable RAM sockets (see Figure 2-3)
W9	1-2	=Processor's clock input connected to STD BUS CNTRL* line. Crystal must be removed.
	3-4	=Processor's clock input connected to external clock input EXT CLK J1-8. Crystal must be removed.
	no jumper	=Processor's clock input generated on card
	5-6	Not used
W10		For Pro-Log use only

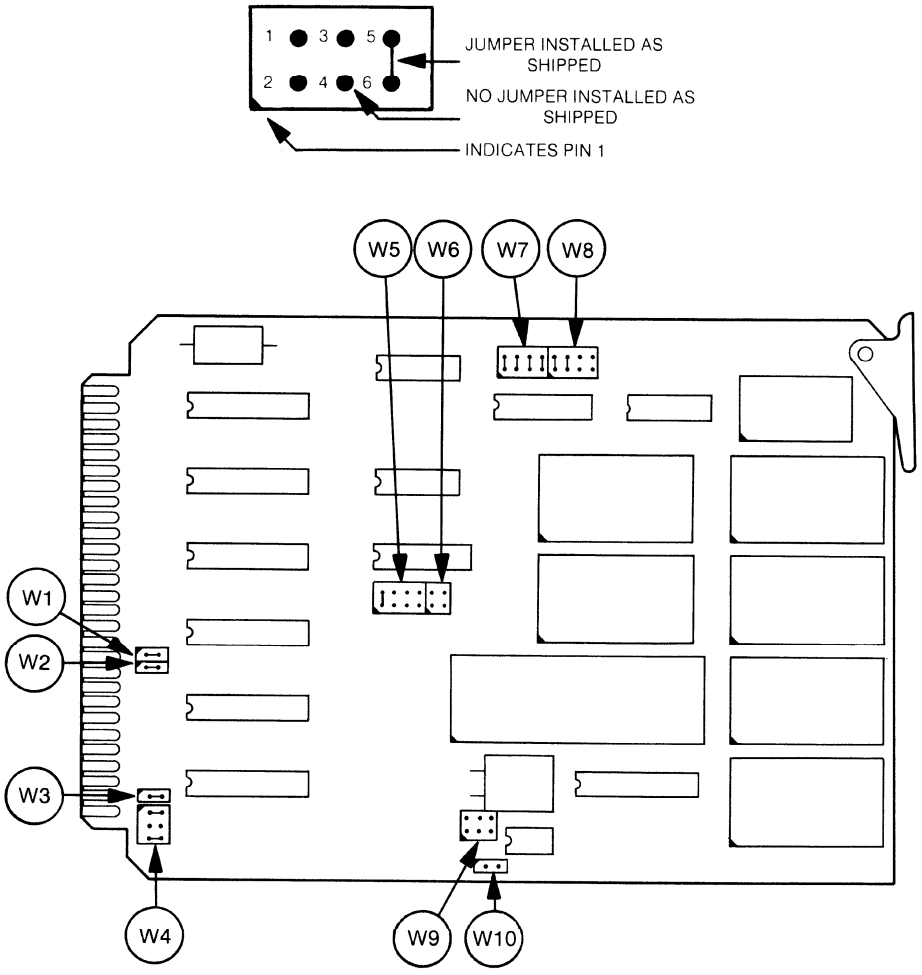
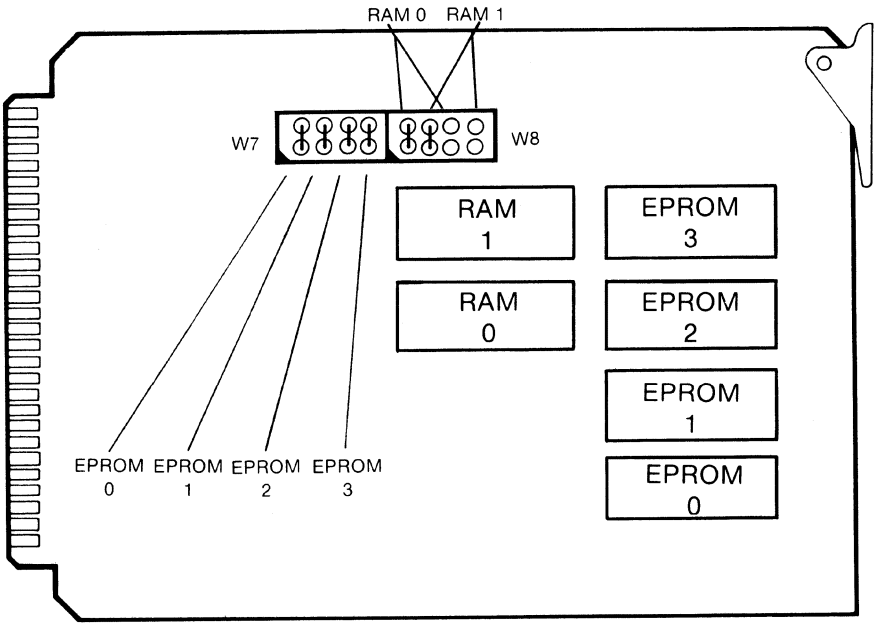


Figure 2-2. Jumper Locations and Functions (7805)



NOTE 1: Jumpers W7 and W8 are shown in the as-shipped condition.
2: To disable a RAM, both jumpers indicated must be removed.

Figure 2-3. Chip Disable Jumpers (7805)

PART	MANUFACTURER PART NUMBER	
	ELCO CORP.	BERG ELECTRONICS
2-PIN HEADER	00 8261 02 32 00 852	65611-102
4-PIN HEADER	00 8261 04 32 00 852	65611-104
6-PIN HEADER	00 8261 06 32 00 852	65611-106
8-PIN HEADER	00 8261 08 32 00 852	65611-108
CONNECTOR	00 8261 02 42 00 870	—

Figure 2-4. Wire Jumper Replacements (7805)

MEMORY MAPPING

The 7805 Processor Card contains two sockets for 2Kx8 byte-wide RAM and four sockets for 2Kx8 EPROMs (2716 type). One 2Kx8 byte-wide RAM chip is provided by Pro-Log. Jumper blocks W7 and W8 are provided to disable any unused memory sockets. Memory addresses normally occupied by the unused sockets can then be designated to devices outside the 7805.

The 7805 can be mapped to any one of the four 16K quadrants addressable by a 16-bit microprocessor. The card itself will only occupy 12K of the 16K available. The remaining 4K can be occupied by external memory devices. For example, the card as shipped can be mapped 0000 to 3FFF. This configuration leaves 3000 to 3FFF available for external memory.

The 7805 has another memory addressing option which allows a user to address onboard RAM to the last 4K of memory space within the 16K quadrant. In such a case, the space that RAM would normally occupy would then become open to external memory. Jumper Block W5 controls the quadrant that the 7805 onboard memory resides in. Figure 2-5 describes the memory addressing options for the 7805.

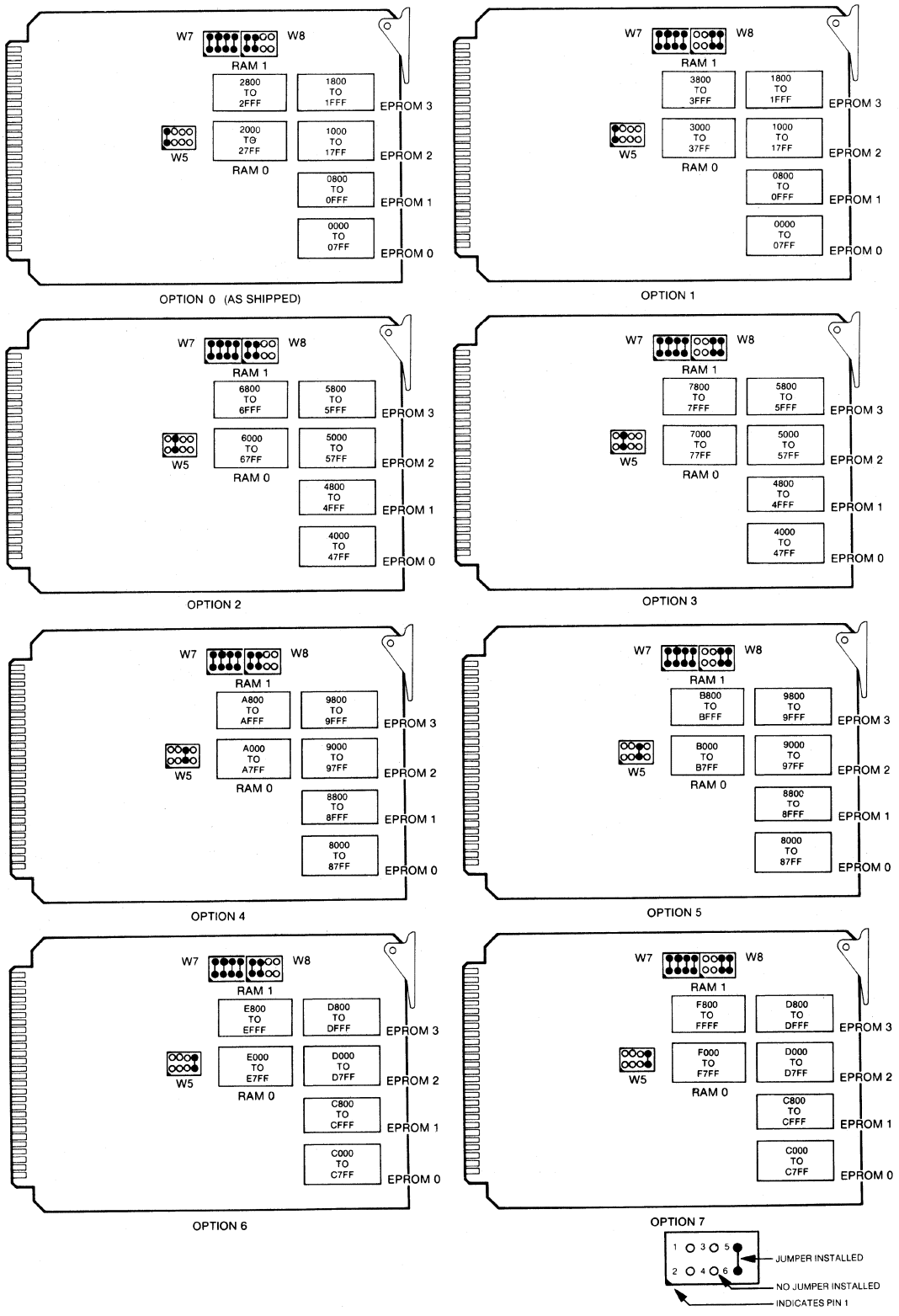


Figure 2-5. Memory Addressing Options (7805)

MEMORY TYPES

The 7805 Processor Card uses two different kinds of memory: 2K RAMs and 2K EPROMs. Figure 2-6 is a list of components which are compatible for use on the 7805 card. If you wish to use other memory components, compare the manufacturer's data sheets to the socket configurations. Also, check their data sheets for any special requirements.

CHIP #	ORGANIZATION	nS
Intel Corporation		
21812	2K SRAM	150
*2716	2K EPROM	350-450
Mostek Corporation		
MK34000	2K ROM	350
*MK2716	2K EPROM	300
MK4082	2K SRAM	
National Semiconductor		
*MM2716	2K EPROM	350-450
Motorola		
*MCM2716	2K EPROM	250-450
Texas Instruments		
*TMS2516	2K EPROM	
Mitsubishi		
*M58725	2K EPROM	200
NEC Microcomputers		
*μPD2716	2K EPROM	450
American Microsystems (AMI)		
S4028	2K SRAM	200
Synertek		
*SY2716	2K EPROM	350-450
OKI		
*MSM5128	2K SRAM	150-200-250
Toshiba		
*TMM2016	2K SRAM	150-250

*Recommended Devices

Figure 2-6. Suggested Memory Devices (7805)

MEMEX

The MEMEX signal line is part of the STD BUS. It is used as a memory bank select line. It is possible to have two banks of memory, each with up to 64K bytes, in a system. One bank would be enabled when MEMEX is high, and the other when MEMEX is low. Pro-Log memory cards include the MEMEX line in their address decoding.

There are several jumper options affecting MEMEX. Jumper W1 determines whether MEMEX will be grounded, or if it will be left floating for another card in the system to control. As shipped, it is grounded. Jumper W6 determines how onboard memory will respond to MEMEX. Jumper 1-2 causes onboard memory to respond to MEMEX high and pulls up MEMEX in the event that it is not driven. Jumper 3-4 causes onboard memory to respond to MEMEX low. No jumper (as shipped) leaves onboard memory independent of MEMEX. See Figure 2-2 for the physical location of these jumper blocks.

As shipped, jumper block W6 has no jumpers installed. The pull-up resistor causes onboard memory to be permanently enabled.

IOEXP

The IOEXP line is one of the STD BUS standard signals. It is used to select between different banks of input and output ports. The 7805 does not control the IOEXP line. IOEXP is grounded on the 7805 through jumper W2. If another card needs control of the IOEXP line, jumper W2 can be removed. This will leave the line floating. See Figure 2-2 for the physical location of jumper W2.

J1 16-PIN DIP SOCKET

The 7805's socket J1 allows the user to gain access to several of the pins on the 8085A processor chip (see Figure 2-7). Pins 1 through 3 allow the user to implement the vectored interrupt pins on the processor. Pins 4 and 5 are connected to the processor's SID and SOD pins, allowing the user to create a serial port directly into the processor. Pins 6 and 7 are spares and pin 8 is an external clock input. Pins 9 through 16 are grounded. Figure 2-8 describes the loading characteristics of the J1 socket.

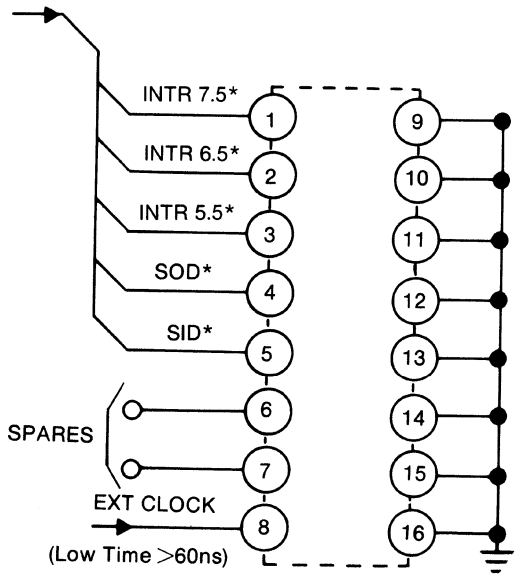


Figure 2-7. The J1 16-Pin Socket (7805)

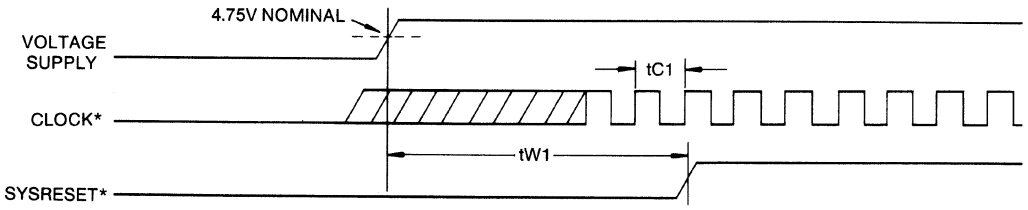
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)							INPUT (LSTTL LOADS)
MNEMONIC							MNEMONIC
Interrupt 7.5*	5		1	16	OUT		Ground
Interrupt 6.5*	5		2	15	OUT		Ground
Interrupt 5.5*	5		3	14	OUT		Ground
SOD*		15	4	13	OUT		Ground
SID*	5		5	12	OUT		Ground
(Spare)			6	11	OUT		Ground
(Spare)			7	10	OUT		Ground
External Clock	5		8	9	OUT		Ground

*Designates Active Low-Level Logic

Figure 2-8. Load Characteristics and Pinouts for the J1 Connector (7805)

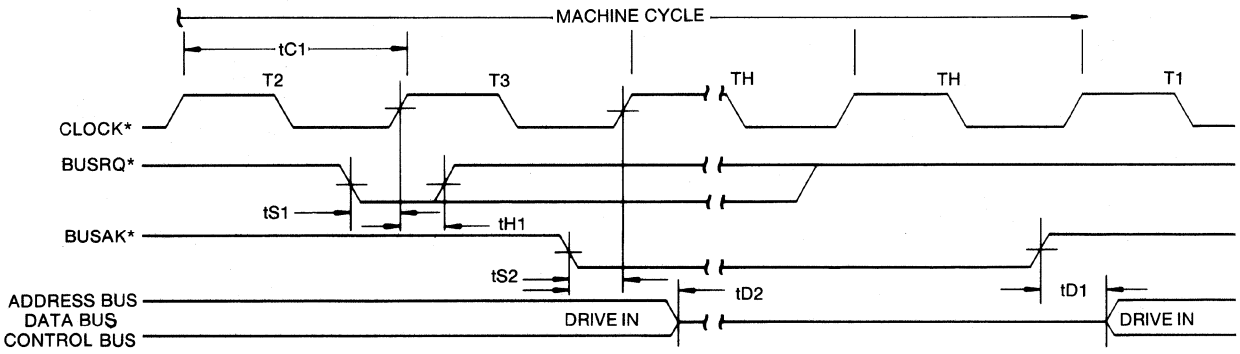
TIMING SPECIFICATIONS

Figures 2-9 through 2-13 show the signal sequences and timing for various 7805 functions. They show the signals as they appear at the card edge connector of the 7805.



SYMBOL	PARAMETER	6.25 MHz		6.144 MHz		UNITS
		MIN	MAX	MIN	MAX	
tC1	Clock Cycle Time		320		325	ms
tW1	Power up reset width after supply threshhold	12	60	12	60	ms

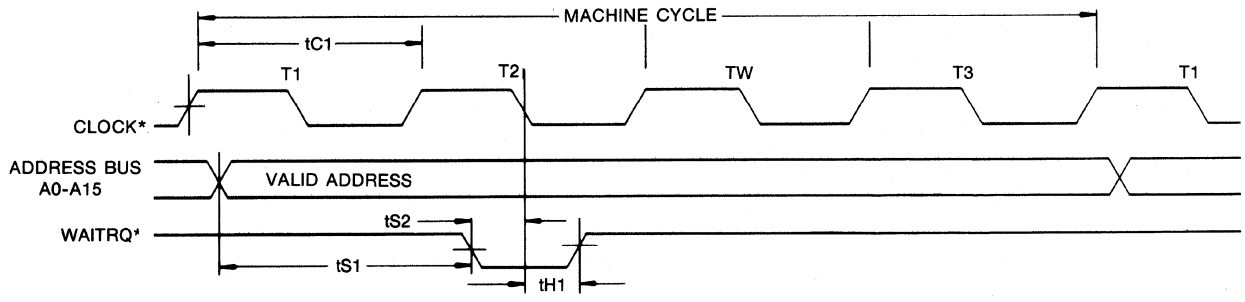
Figure 2-9. Reset After Power-up (7805)



SYMBOL	PARAMETER	6.25 MHz		6.144 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock Cycle Time		320		325
tD1	Bus delay after BUSAK* high		240		240
tD2	Bus delay after BUSAK* low		45		45
tH1	BUSRQ* hold after start of T3	0		0	
tS1	BUSRQ* setup prior to T3	200		200	
tS2	BUSAK* setup prior to TH	115		120	

All times given in nanoseconds

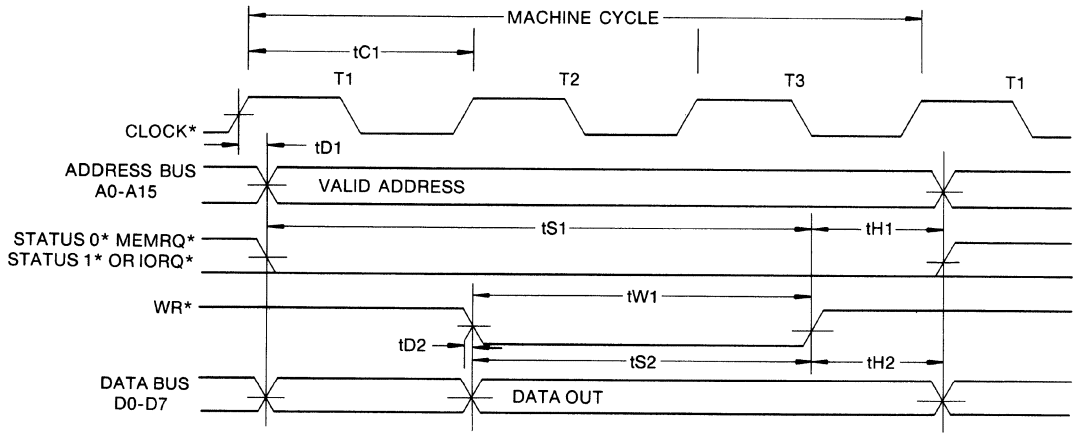
Figure 2-10. BUS Request Timing (7805)



SYMBOL	PARAMETER	6.25 MHz		6.144 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock Cycle Time		320		325
tH1	WAITRQ* hold time after T2/TW	0		0	
tS1	Address setup before WAITRQ*		185		190
tS2	WAITRQ* setup before T2/TW	110		110	

All times given in nanoseconds

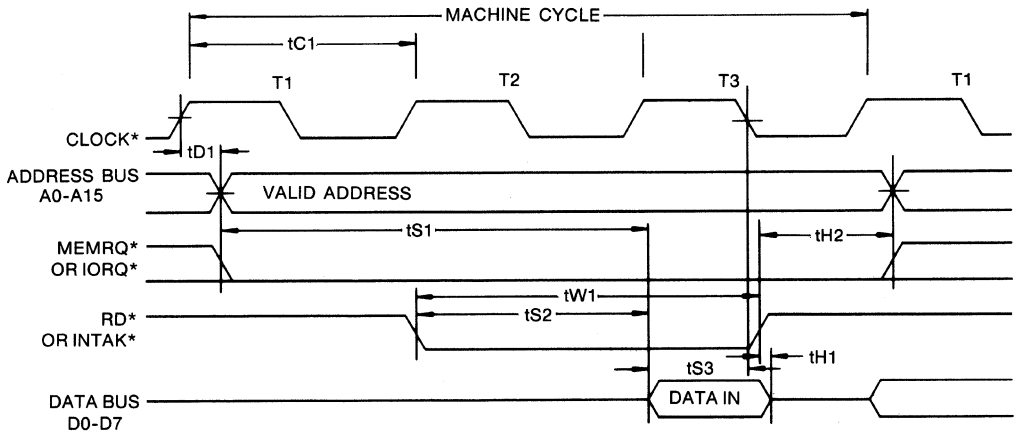
Figure 2-11. Wait Request Timing (7805)



SYMBOL	PARAMETER	6.25 MHz		6.144 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock Cycle Time		320		325
tD1	Address delay from T1 clock		145		145
tD2	Data delay from WR*	65		65	
tH1	Address hold time	90		90	
tH2	Data hold time	65		65	
tS1	Address setup before write strobe	625		635	
tS2	Data setup time before write strobe	400		400	
tW1	WR* pulse width	400		400	

All times given in nanoseconds

Figure 2-12. Write Timing: Memory Write and Output (7805)



SYMBOL	PARAMETER	6.25 MHz		6.144 MHz	
		MIN	MAX	MIN	MAX
tC1	Clock Cycle Time		320		325
tD1	Address delay from T1 clock		155		155
tH1	Data hold time	0		0	
tH2	Hold time after RD*	135		135	
tS1	Address setup before data valid		540		555
tS2	RD* setup before data valid		270		280
tS3	Data setup time	100		100	
tW1	RD* pulse width	390		375	

All times given in nanoseconds

Figure 2-13. Read Timing: Memory Read, Input and Interrupt (7805)

POWER-ON AND PUSH-BUTTON RESET

Power-on reset holds the SYSRESET* line low and releases it a maximum of 60ms after the VCC reaches 4.75V. The PBRESET* is debounced approximately 20ms, and produces a maximum 40ms SYSRESET* pulse.

SPECIFICATIONS

Figure 2-14 shows the electrical specifications for the 7805. Environmental and power specifications are shown in Figures 2-15 and 2-16. Figure 2-17 gives the pinout and loading characteristics of the connection between the 7805 and the STD BUS.

MNEM.	PARAMETER	Recommended Operating Limits			Absolute Non-Operating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
Vcc	Logic supply	4.75	5.00	5.25	0	5.50	Volts

Figure 2-14. Electrical Specifications (7805)

MNEM.	PARAMETER	Recommended Operating Limits			Absolute Non-Operating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
—	Free Air Temperature	0	+25	+55	-40	+75	°C
—	Humidity	5	—	95[1]	5	95[1]	%RH

[1] Non condensing relative humidity

Figure 2-15. Environmental Specifications (7805)

MNEM.	PARAMETER	Recommended Operating Limits			
		MIN	TYP	MAX	UNITS
Icc[1]	Vcc Supply Current		460	780	mA

[1]Icc specification assumes that one 2Kx8 RAM socket is loaded (as shipped). For maximum memory currents: add 60 mA selected, 7 mA standby per 2Kx8 static CMOS RAM (OKI MSM 5128 type), add 120 mA selected, 30 mA standby per 2Kx8 static RAM (OKI MSM 2128 type) and 100 mA selected, 25mA standby per 2Kx8 EPROM (Intel 2716 type).

Figure 2-16. Electrical Specifications Over Operating Range (7805)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	50	8	7	50	5	D3
D6	5	50	10	9	50	5	D2
D5	5	50	12	11	50	5	D1
D4	5	50	14	13	50	5	D0
A15	5	50	16	15	50	5	A7
A14	5	50	18	17	50	5	A6
A13	5	50	20	19	50	5	A5
A12	5	50	22	21	50	5	A4
A11	5	50	24	23	50	5	A3
A10	5	50	26	25	50	5	A2
A9	5	50	28	27	50	5	A1
A8	5	50	30	29	50	5	A0
RD*	5	50	32	31	50	5	WR*
MEMRQ*	5	50	34	33	50	5	IORQ*
MEMEX (GROUND)	5	OUT	36	35	OUT		IOEXP (GROUND)
MCSYNC* (ALE*)	5	50	38	37			REFRESH*
STATUS 0*(S0*)	5	50	40	39	50	5	STATUS 1* (S1*)
BUSRQ*(HOLD*)	5		42	41	50	5	BUSAK* (HLDA*)
INTRQ*(INTR*)	5		44	43	50	5	INTAK* (INTA*)
NMIRQ*(TRAP*)	5		46	45		15	WAITRQ* (READY)
PBRESET*(R*)	(1)		48	47	50	5	SYSRESET* (RST*)
CNTRL*(EXT CLK IN)	IN		50	49	50		CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

(1) Switch Input
* Designates active low-level logic
( ) Designates equivalent 8085A pin names

Figure 2-17. STD BUS Edge Connector Pin List (7805)

SECTION 3
Operation and Programming

Section 3 normally contains instructions for operating and programming of Pro-Log Series 7000 STD BUS cards. The 7805 requires no special operating instructions.

SECTION 4
Operating Software

Section 4 normally contains software subroutines to aid in using Pro-Log Series 7000 STD BUS cards. The 7805 card requires no special operating software.

SECTION 5
Maintenance

The 7805 Card does not require scheduled maintenance. If you have a problem with the card, call our Customer Support group (see "Return for Repair Procedure"). For detailed information on the card's circuitry, refer to the schematic and assembly drawings shipped with the card.

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call our factory direct at (408) 372-4593, and ask for CUSTOMER SUPPORT.
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

> **CAUTION:** Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during shipment. Use conductive foam pads or conductive plastic bags, and **never** place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.